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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,924	01/13/2004	Joseph C. Fjelstad	SIPI-P113	3742

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EXAMINER	
NASRI, JAVAID H	

ART UNIT	PAPER NUMBER
2839	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,924	FJELSTAD ET AL.	
	Examiner	Art Unit	
	Javaid Nasri	2839	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

    a) On page 3, Para [010], line 2, delete "according to an embodiment", second occurrence.

Appropriate correction is required.

Claim Objections

2. Claims 18-20 are objected to because of the following informalities:

    a) In claims 18-20, line 2, change "elements between" to -- elements **is** between --.

    b) In claim 20, line 2, it is not clear between 45 degrees and what?

Appropriate correction is required.

Drawings

3. The drawings received on 10/5/2004 are objected to because figures in general are confusing and are not clear enough to understand the claims properly. If possible, provide numerals in the claims.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Seyama (4,912,603, cited in IDS).

Seyama discloses, **for claim 1**, a board (21); a plurality of devices mounted to the board; a first set of contact points (see figure 8, choose any side contacts) provided adjacent a first side of the board for connecting to a first data bus (see figure 11); a second set of contact points (see figure 8, choose the other side contacts) provided adjacent to a second side of the board for connecting

to a second data bus (see figure 11); a plurality of signal paths provided on the board (see figure 8), each signal path extending between a first contact point in the first set and a second contact point in the second set (see figure 8, depends which contacts are chosen); wherein each of the plurality of signal paths has substantially an identical length and a same number of turns on the board, **for claim 2**, each of the plurality of signal paths includes a number of turns that is less than two, **for claim 3**, the board includes a bottom edge that is configured to be edge-mounted to a substrate, and wherein one of the first set of contact points for at least some of the plurality of signal paths is provided adjacent to the bottom edge and proximate to one of the lateral sides, and wherein for each of the contact points provided adjacent to the bottom edge and proximate to one of the lateral sides, a corresponding signal path has two turns on the board (see figure 10), **for claims 4 and 11**, the board includes a bottom edge that is configured to be edge-mounted to a substrate, and a pair of lateral sides that extend from the bottom edge, and wherein each contact point in the first set of contact points is provided on or adjacent to one of the lateral sides, and wherein for each contact point in the first set, a corresponding signal path extends to a corresponding contact point in the second set, and wherein said corresponding signal path has less than two turns on the board, **for claims 5 and 12**, for each contact point in the first set, the corresponding signal path that extends to the corresponding contact point in the second set has zero turns on the board (see figure 8), **for claim 6**, at least some of the plurality of components are memory devices, **for claim 7**, a set of one or more boards (21) upon which the plurality of memory devices are provided, wherein the set includes at least a first board on which at least some of the plurality of memory devices are provided, a plurality signal paths provided on the first board (see figure 8), wherein each signal path in the plurality of signal paths includes a first

set of contact points (choose any contact as first set, see figure 8) that interconnect the first board to the controller from a position that is proximate to a first lateral side of the first board, and a second set of contact points (choose other contacts as second set) that interconnect the board to another component from another position that is proximate to a second lateral side of the first board, and wherein each of the plurality of signal paths has a substantially identical length and an identical number of turns between a contact point in the first set of contact points and a contact point in the second set of contact points; and a bus (76, 77) connected to the first set of contact points and communicatively coupled to the controller, **for claim 8**, the bus is provided through a flex cable (76, 77), **for claim 9**, an end of the flex cable is directly connected to the controller, (see figure 8), **for claim 10**, the first board is edge-mounted to motherboard (1) on a bottom side (bottom is a relative term), and wherein a contact point in the first set of contact points for at least some of the plurality of signal paths is provided adjacent to a bottom edge, and wherein for each contact point provided adjacent to the bottom edge, the signal path of that contact point has two turns on the board (see figure 11), **for claim 13**, a motherboard (1) upon which the controller and the set of one or more boards (21) are mounted, and wherein the bus (76, 77) is external to the motherboard, **for claim 14**, the first board (21) is connected to a second board (1) in the set via a second bus (76, 77) provided on a flex cable, **for claim 15**, the first board and the second board are each mounted to a motherboard (2).

6. Claims 16-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (4,095,866, cited in IDS).

Merrill discloses, **for claim 16**, a first segment (at 16); a second segment (at 18); an opening formed between the first segment and the second segment (see figure 1), wherein the opening is

dimensioned to receive the substrate (20); wherein at least one of the first segment and the second segment includes a plurality of connector members (22, 24, 26, 28), each of the at least one connector members being positioned to extend electrical contact from a point on the substrate to a tip of that connector member that extends into the opening (see figure 1), wherein each of the at least one of the plurality of connector elements has a majority of its length be substantially linear and is angled with respect to a plane of the substrate (see figure 1), **for claim 17**, a substantial portion of the at least one of the plurality of connector elements is linear (see figure 1), **for claims 18-20**, a substantial portion of the at least one of the plurality of connector elements is between 20 and 70/30 and 60/45 degrees with respect to the plane of the substrate (depends from which part of the connector the angle is measured), **for claim 21**, a board (14) upon which the plurality of memory devices are provided, a connector that couples the board to a substrate (20), wherein the connector comprises: a first segment (16); a second segment (18); opening formed between the first segment and the second segment, wherein the opening is dimensioned to receive the substrate (20), wherein at least one of the first segment and the second segment includes a plurality of connector members (22. 24, 26, 28), each of the at least one connector members being positioned to extend electrical contact from a point on the substrate to a tip of that connector member that extends into the opening; wherein each of the at least one of the plurality of connector elements has a majority of its length be substantially linear and is angled with respect to a plane of the substrate; and wherein the connector extends communications from the controller to the board, **for claim 22**, the connector includes a mechanism for extending a bus embedded within a cable (not shown) from the controller to the board.

7. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Dougherty et al. (4,202,007, cited in IDS).

Dougherty et al. discloses, **for claim 1**, a board (see figure 8B, 8C); a plurality of devices mounted to the board; a first set of contact points (see figure 8B, 8C), choose any side contacts) provided adjacent a first side of the board for connecting to a first data bus (25); a second set of contact points (see figure 8B, 8C, choose the other side contacts) provided adjacent to a second side of the board for connecting to a second data bus (25); a plurality of signal paths provided on the board), each signal path extending between a first contact point in the first set and a second contact point in the second set (see figure 8B, 8C, depends which contacts are chosen); wherein each of the plurality of signal paths has substantially an identical length and a same number of turns on the board, **for claim 2**, each of the plurality of signal paths includes a number of turns that is less than two, **for claim 3**, the board includes a bottom edge that is configured to be edge-mounted to a substrate, and wherein one of the first set of contact points for at least some of the plurality of signal paths is provided adjacent to the bottom edge and proximate to one of the lateral sides, and wherein for each of the contact points provided adjacent to the bottom edge and proximate to one of the lateral sides, a corresponding signal path has two turns on the board (see figure 8B), **for claims 4 and 11**, the board includes a bottom edge that is configured to be edge-mounted to a substrate, and a pair of lateral sides that extend from the bottom edge, and wherein each contact point in the first set of contact points is provided on or adjacent to one of the lateral sides, and wherein for each contact point in the first set, a corresponding signal path extends to a corresponding contact point in the second set, and wherein said corresponding signal path has less than two turns on the board, **for claims 5 and 12**, for each contact point in the first set, the

corresponding signal path that extends to the corresponding contact point in the second set has zero turns on the board (see figure 8B, not numbered), **for claim 6**, at least some of the plurality of components are memory devices, **for claim 7**, a set of one or more boards (see figures 1, 3A, 3B, 5, 6, 8B,) upon which the plurality of memory devices are provided, wherein the set includes at least a first board on which at least some of the plurality of memory devices are provided, a plurality signal paths provided on the first board, wherein each signal path in the plurality of signal paths includes a first set of contact points (choose any contact as first set, see figure 8B, 8C) that interconnect the first board to the controller from a position that is proximate to a first lateral side of the first board, and a second set of contact points (choose other contacts as second set) that interconnect the board to another component from another position that is proximate to a second lateral side of the first board, and wherein each of the plurality of signal paths has a substantially identical length and an identical number of turns between a contact point in the first set of contact points and a contact point in the second set of contact points; and a bus (25) connected to the first set of contact points and communicatively coupled to the controller, **for claim 8**, the bus is provided through a flex cable (not shown), **for claim 9**, an end of the flex cable is directly connected to the controller, (not shown), **for claim 10**, the first board is edge-mounted to motherboard (see figure 6) on a bottom side, and wherein a contact point in the first set of contact points for at least some of the plurality of signal paths is provided adjacent to a bottom edge, and wherein for each contact point provided adjacent to the bottom edge, the signal path of that contact point has two turns on the board, **for claim 13**, a motherboard (see figure 6) upon which the controller and the set of one or more boards (see figure 6) are mounted, and wherein the bus (25) is external to the motherboard, **for claim 14**, the first board is connected to

a second board in the set via a second bus (see figure 3A) provided on a flex cable (not shown), **for claim 15**, the first board and the second board are each mounted to a motherboard (see figure 6).

Contact

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javaid Nasri whose telephone number is 571 272 2095. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tulsidas C. Patel can be reached on 571 272 2800 ext 39. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any correspondence to this action may be mailed to:

Commissioner for Patents
Post Office Box 1450
Alexandria, VA 22313-1450

For additional information regarding this new address, which was effective May 1, 2003, see *Correspondence with the United States Patent and Trademark Office, 68 Fed. Reg. 14332 (March 25, 2003).*

Or faxed to: 703-308-7722 or 308-7724 (informal or draft communications should be clearly labeled "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to:

Crystal Plaza 4, Fourth Floor (receptionist)

2201 South Clark Place, Arlington, Virginia

Javaid Nasri
Primary Examiner
Art Unit 2839

JN
Jhn
February 24, 2005